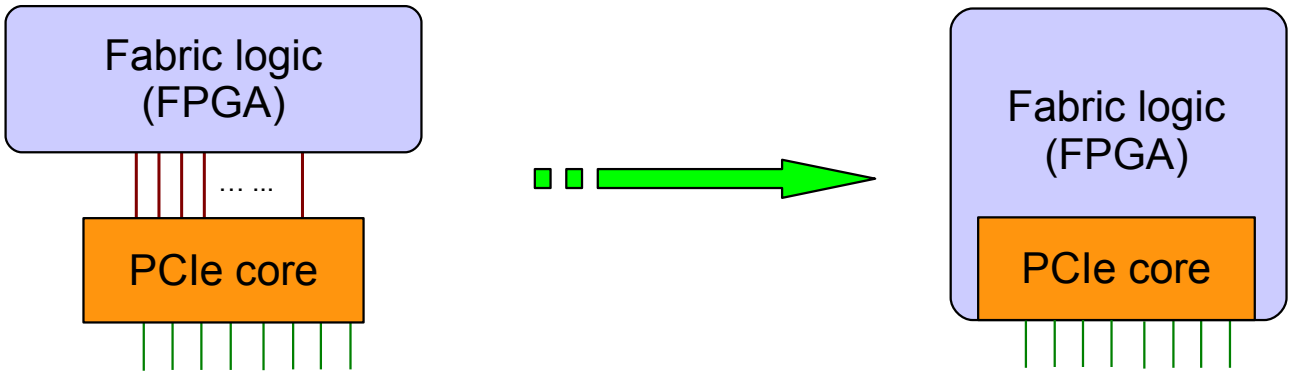
DPR over PCIe

- DPR on Virtex5 & Virtex6
- PlanAhead 12
- ICAP
- PCI Express Gen1
- ChipScope

– Wenxue Gao, 5 May 2011, FPGA-CC

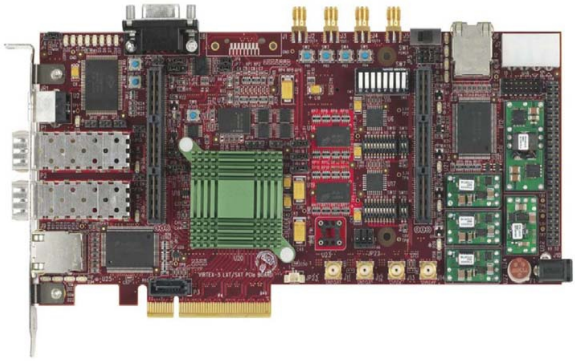
Why DPR?

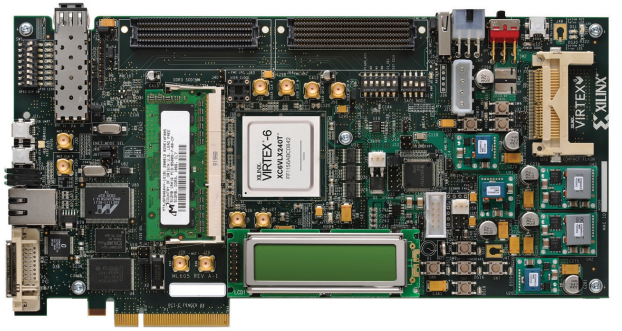
- PCIe should always be alive
- Avoid off-chip interconnection
- Faster FPGA booting
- HW modules treated as SW ones



Overview

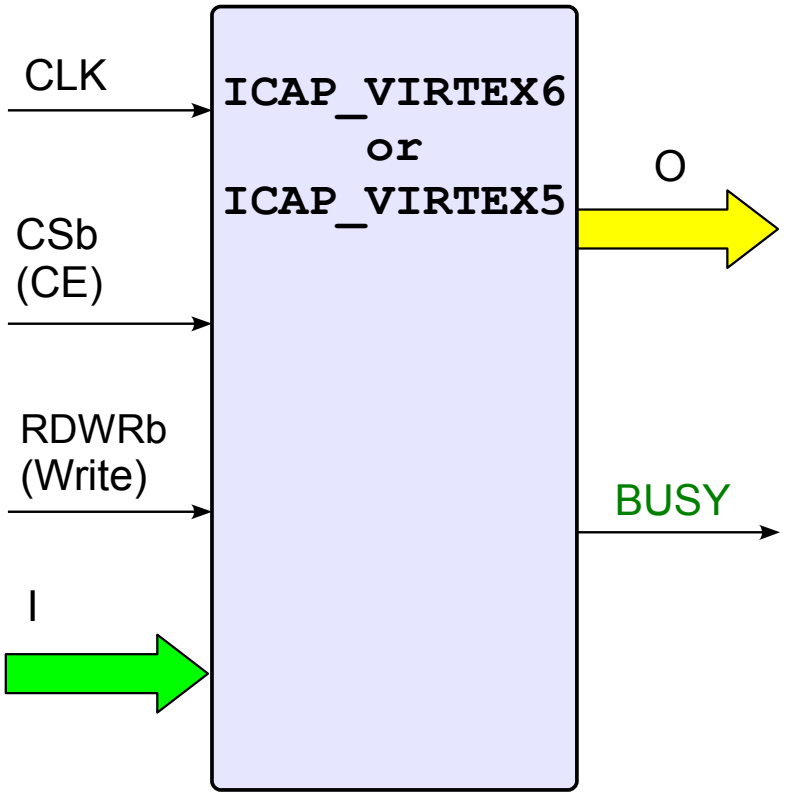
- PlanAhead 12.4
- Boundary decoupling instead of bus-macros
- Enable control along the boundary be manually done
- Reference: XUP examples
- ICAP to PCIe
- Target boards
  - AVNET: Virtex5 LX110T
  - ML605: Virtex6 LX240T





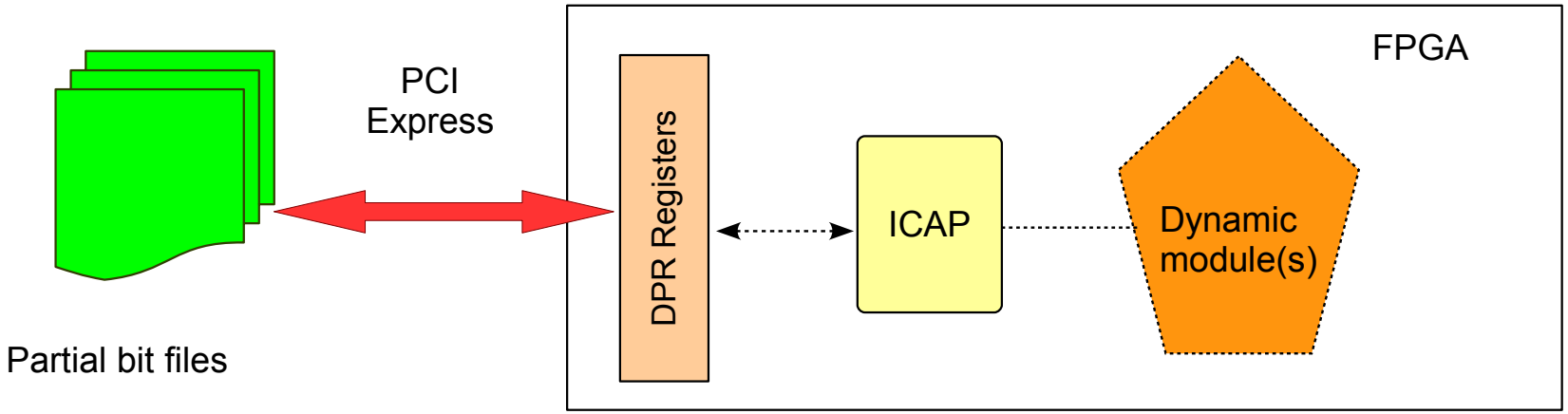
ICAP_VIRTEX6
ICAP_VIRTEX5

- Protocol as **SelectMap**
- Max clock rate 100 MHz
- Bus width
  - X **8**
  - X 16 (Virtex6)
  - X 32
- **CSb** (**CE**) mode to inject data
- Bit reverse
- *M[2:0] ≠ "101" ?*



ICAP write via PIO

- Every data (byte) write is completed in 1 PIO
- Over existed PCIe channel



Configuration speed

- Virtex5 : ~ 1.6 MB/s
- Virtex6 : ~ 6.4 MB/s
- **BUSY** not peeked
- JTAG cable only needed for the initial configuration
- PIO configuration rate is supposed about 4 times faster, if 32-bit ICAP is used
- ABB2 DMA write channel is idle, which might be revised to a fast configuration channel with peak bandwidth of **400** MB/s

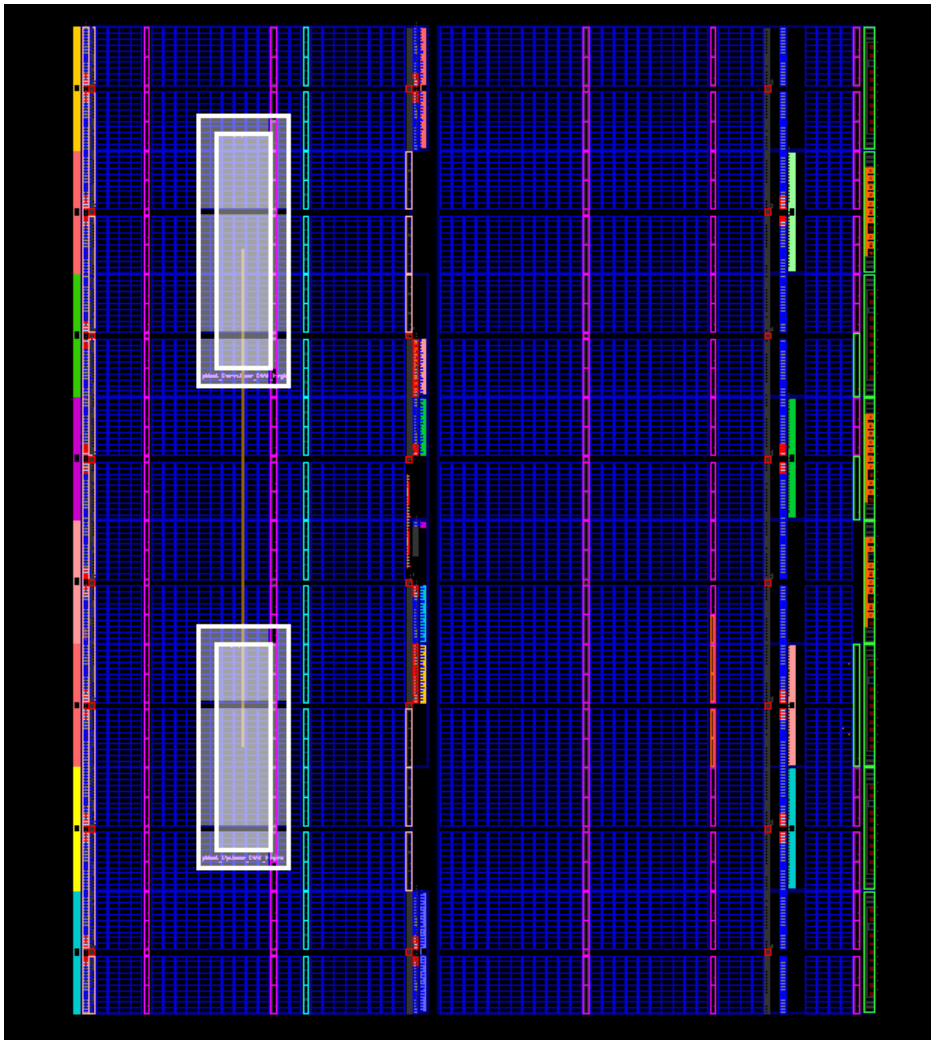
DPR experiments in pairs ...

Virtex5

Virtex6

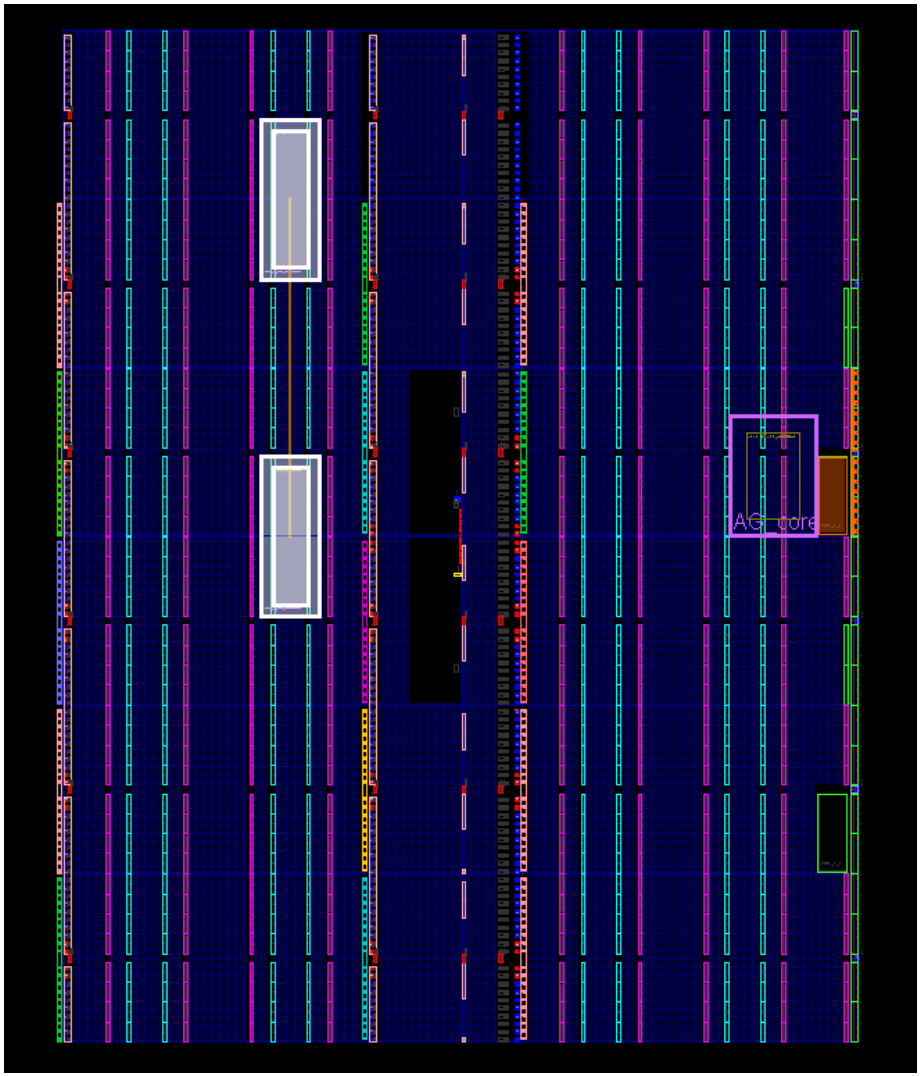
Partitions - Virtex5

- Demo version
- 2 dynamic modules (RMs)
  - DMA read channel
  - DMA write channel
- Every module has 3 versions, including a blank
- Visualized by LED blinking

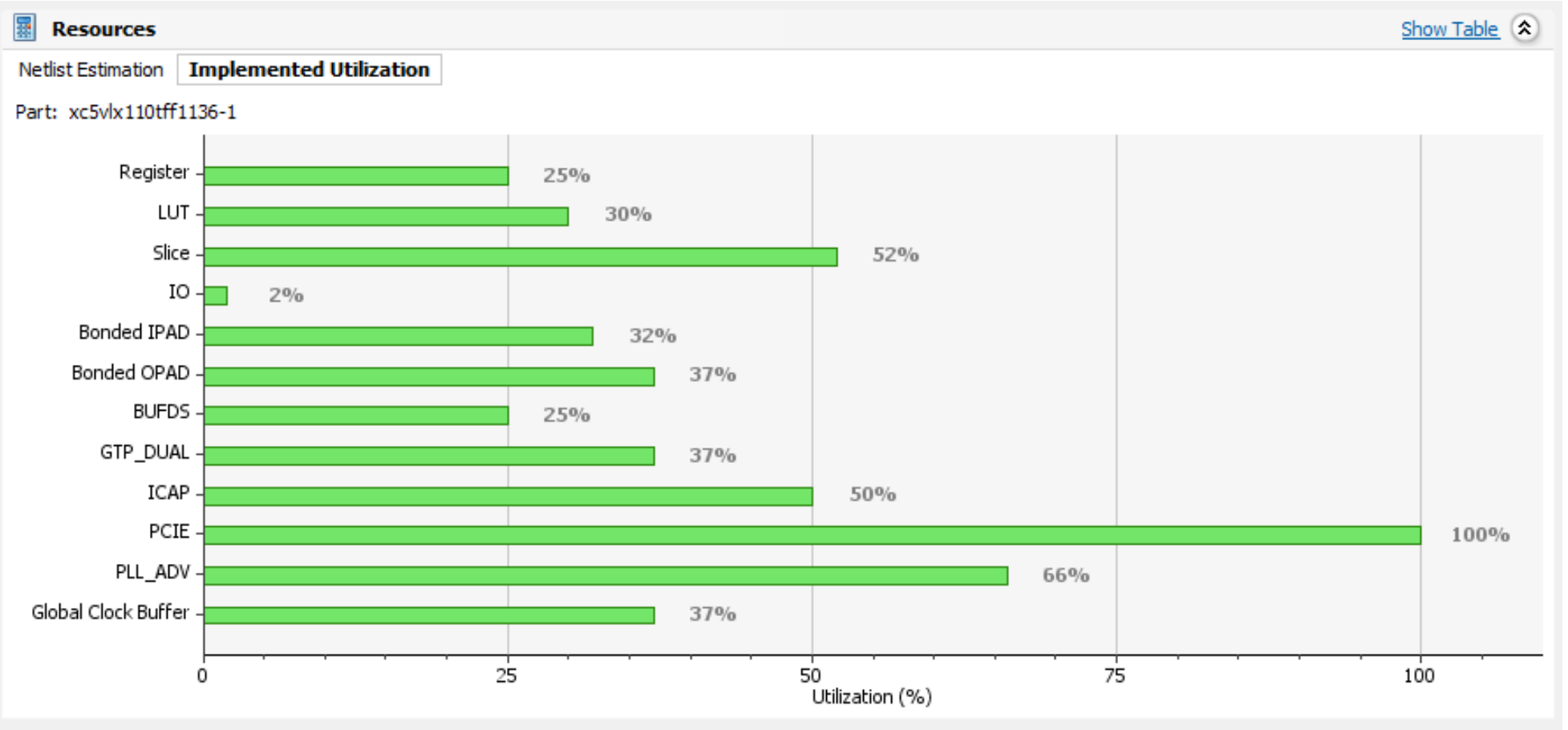


Partitions - Virtex6

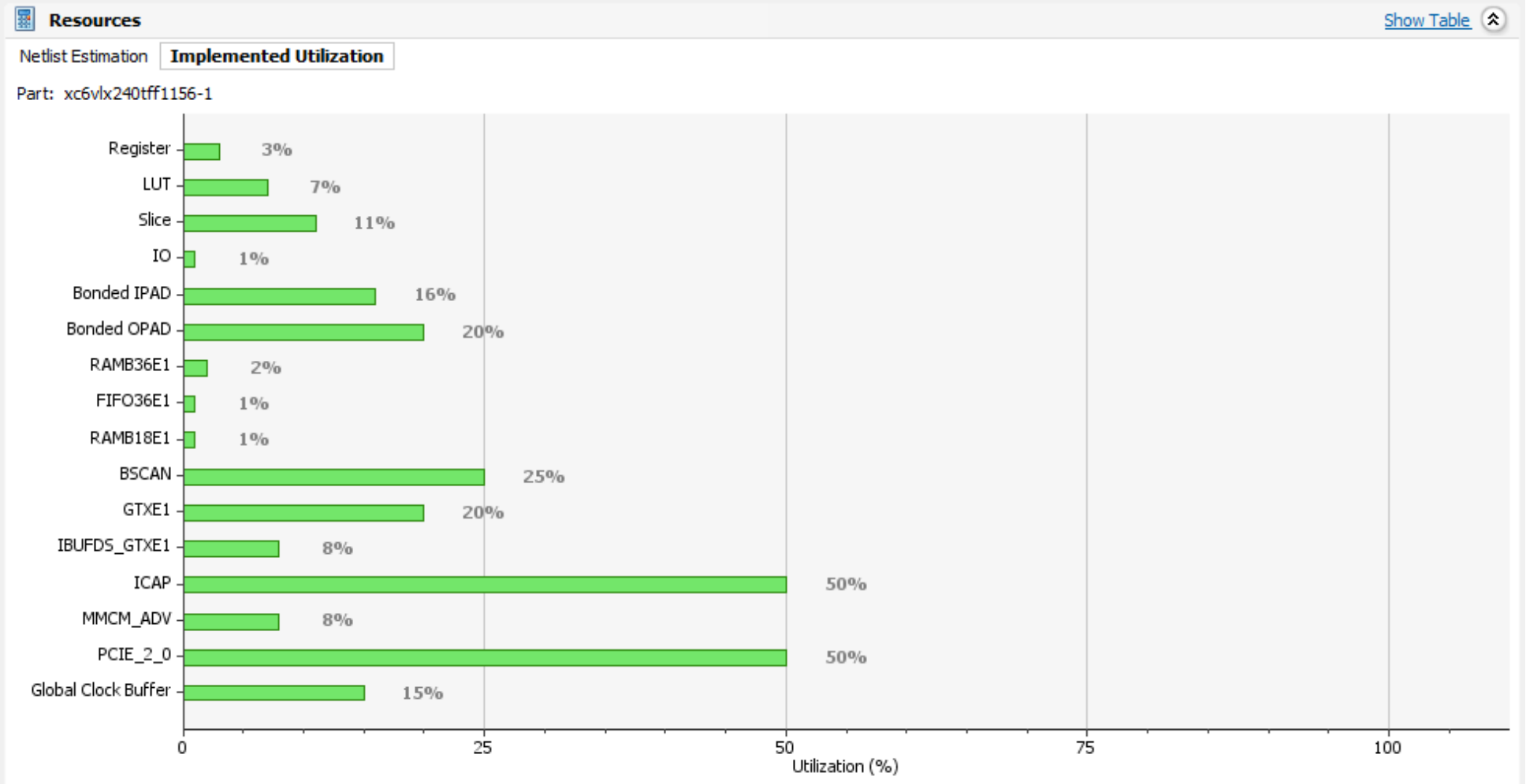
- Demo version
- 2 dynamic modules (RMs)
  - DMA_FSM_ds
  - DMA_FSM_us
- Every module has 3 versions, including a blank
- Visualized by LED blinking



Resource utilization - Virtex5

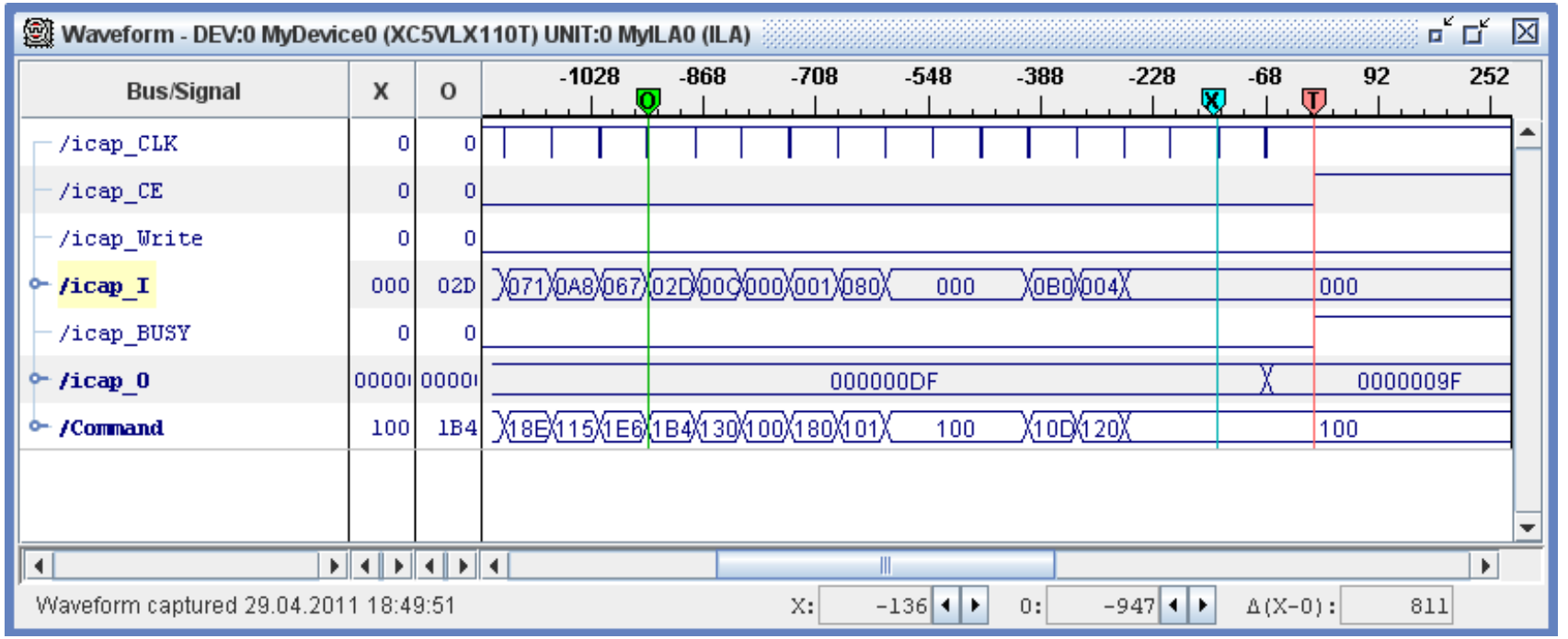


Resource utilization - Virtex6



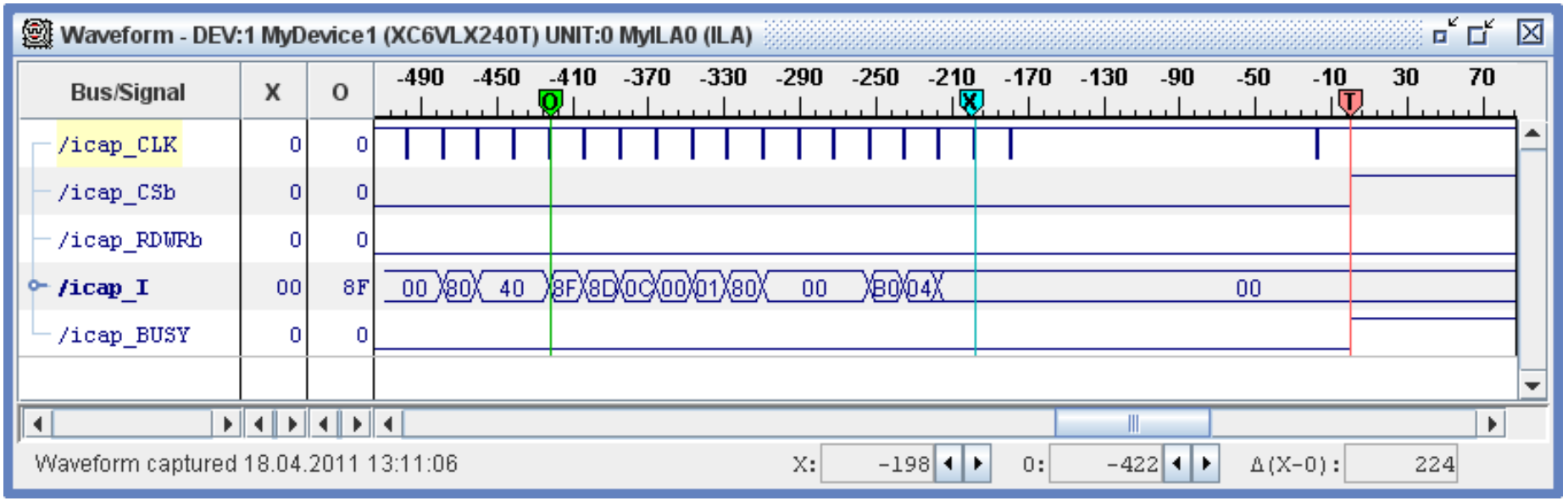
ChipScope view – Virtex5

- Every rising edge of **ICAP_CLK** pushes a data into ICAP
- Estimated peak bandwidth **1.85 MB/s**
  - **12 B/(811 x 8 ns) = 1.85 MB/s**



ChipScope view – Virtex6

- Same infrastructure as of Virtex5
- Estimated peak bandwidth **6.70 MB/s**
  - **12 B/(224 x 8 ns) = 6.70 MB/s**



Console output – Virtex5

```
mp-spirit2:/home/dpr# bin/icap_dpr bitfiles/imp_u1_partial.bit
DPR boundary closed.
DPR in process ...
DPR boundary opened.
DPR successfully finished.
  Bit file name : bitfiles/imp_u1_partial.bit
  Bit file size : 215919 bytes
  Reconfiguration time = 137.948 ms
  Reconfiguration speed = 1.56522 MB/s

mp-spirit2:/home/dpr# bin/icap_dpr bitfiles/imp_d1_partial.bit
DPR boundary closed.
DPR in process ...
DPR boundary opened.
DPR successfully finished.
  Bit file name : bitfiles/imp_d1_partial.bit
  Bit file size : 215919 bytes
  Reconfiguration time = 127.749 ms
  Reconfiguration speed = 1.69019 MB/s
```

< 1.85 MB/s

Console output – Virtex6

```
mp-spirit2:/home/dpr# bin/icap_dpr bitfiles/imp_d2u2_us_partial.bit
DPR boundary closed.
DPR in process ...
DPR boundary opened.
DPR successfully finished.
  Bit file name : bitfiles/imp_d2u2_us_partial.bit
  Bit file size : 136150 bytes
  Reconfiguration time = 21.1862 ms
  Reconfiguration speed = 6.42634 MB/s

mp-spirit2:/home/dpr# bin/icap_dpr bitfiles/imp_d2u2_ds_partial.bit
DPR boundary closed.
DPR in process ...
DPR boundary opened.
DPR successfully finished.
  Bit file name : bitfiles/imp_d2u2_ds_partial.bit
  Bit file size : 136150 bytes
  Reconfiguration time = 22.1401 ms
  Reconfiguration speed = 6.14948 MB/s
```

< 6.70 MB/s

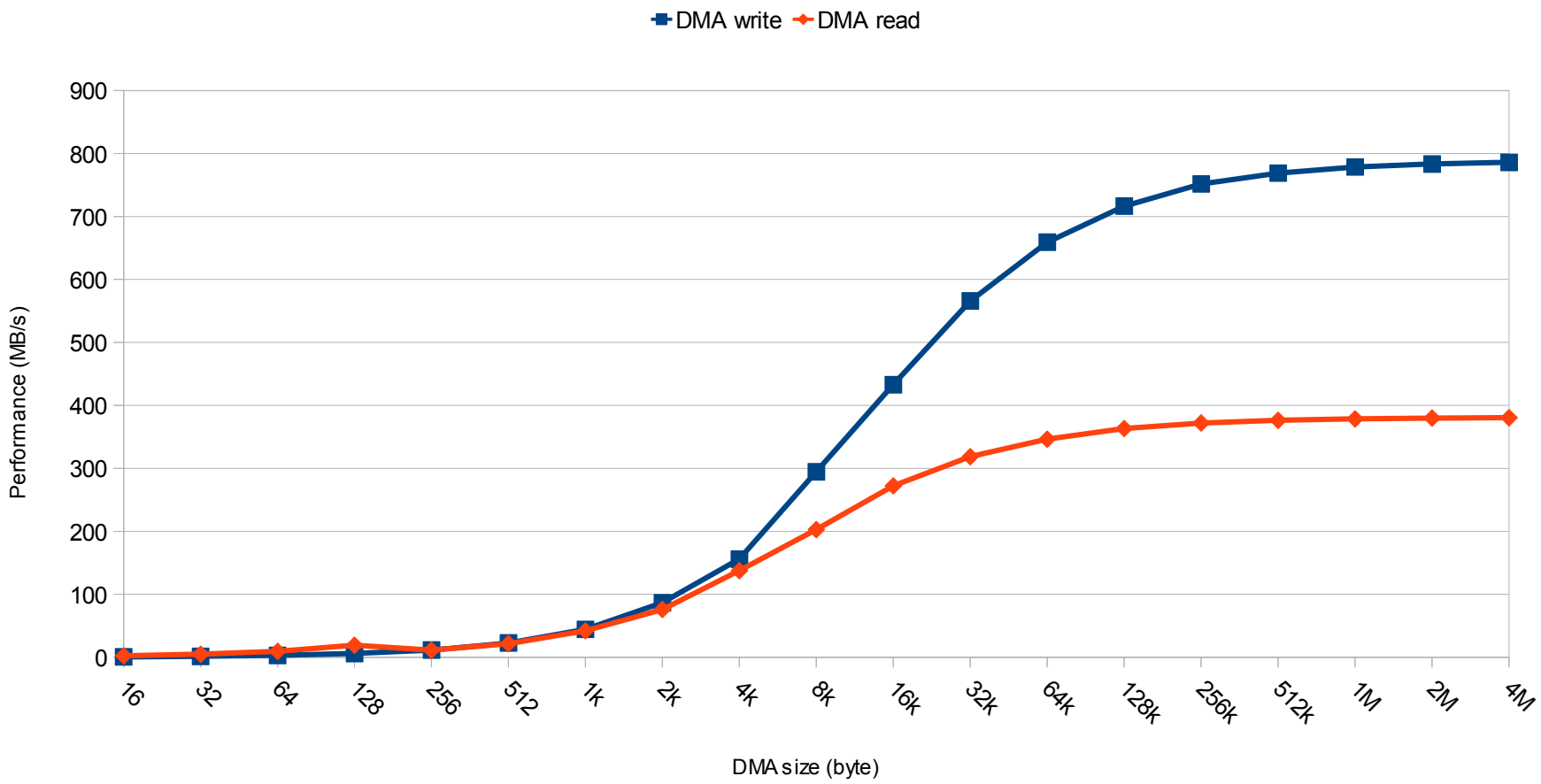
DMA correct – Virtex5

```
mp-spirit2:/home/dpr# bin/mini-write-dma 1|hd; bin/mini-read-dma |hd
00000000  fc aa 69 f0 08 64 5c 17  f8 ae f1 0b f6 dc 3b 82  |..i..d\.......;.|
00000010  9b 5c f6 cf 60 cd 87 5e  f9 63 06 9c 62 27 00 5f  |.\..`..^.c..b'._|
00000020  d1 6a 4f d9 ce ab f0 c7                           |.jO.....|
00000028
00000000  fc aa 69 f0 08 64 5c 17  f8 ae f1 0b f6 dc 3b 82  |..i..d\.......;.|
00000010  9b 5c f6 cf 60 cd 87 5e  f9 63 06 9c 62 27 00 5f  |.\..`..^.c..b'._|
00000020  d1 6a 4f d9 ce ab f0 c7                           |.jO.....|
00000028
```

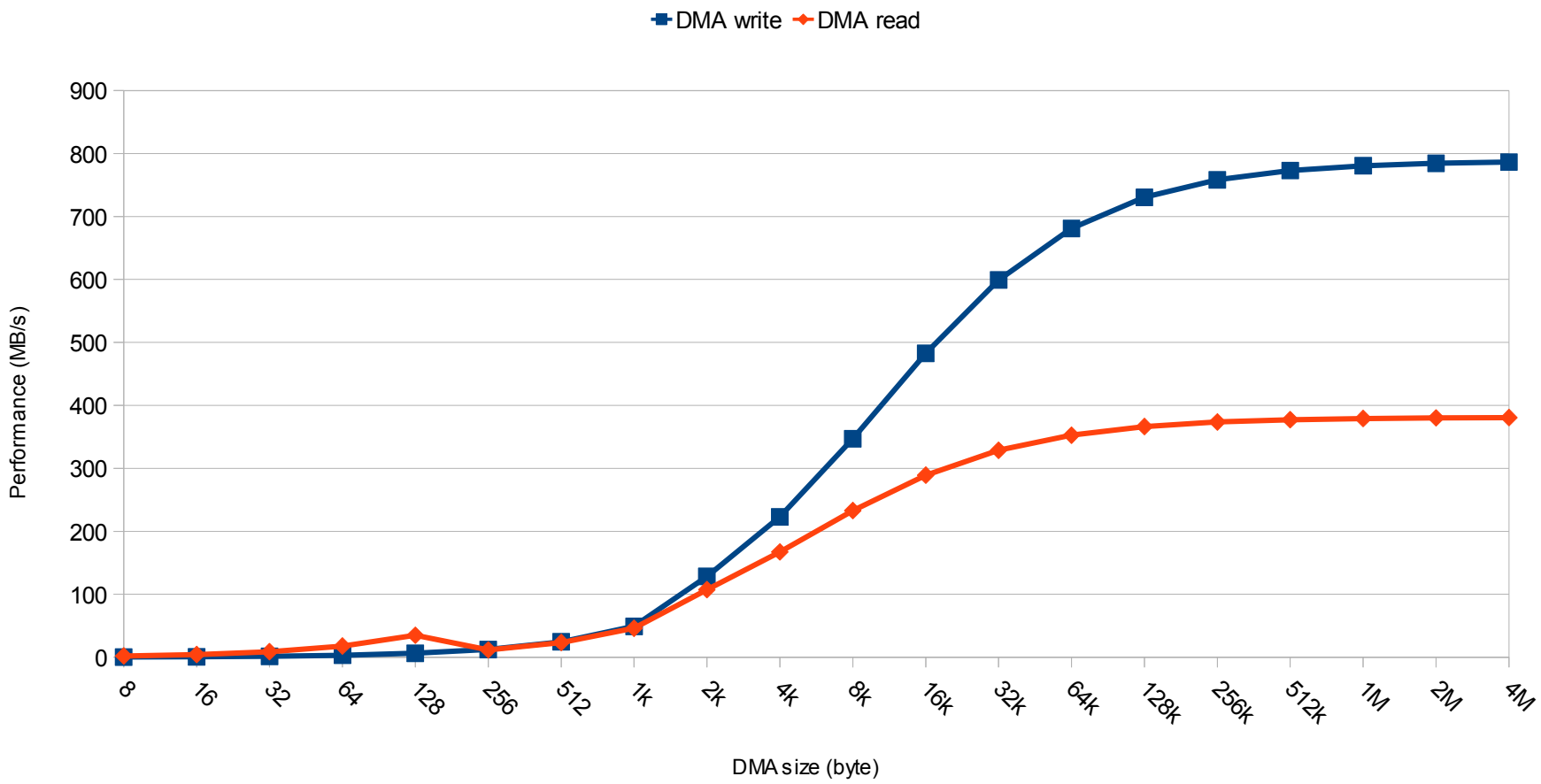
DMA correct – Virtex6

```
mp-spirit2:/home/dpr# bin/mini-write-dma 1|hd; bin/mini-read-dma |hd
00000000  23 08 36 31 86 55 d0 84  07 c4 4c 1b d8 49 fe 6a  |#.61.U....L..I.j|
00000010  1e 43 34 6d f1 e1 05 ff  41 3a 21 6b 26 00 f7 4a  |.C4m....A:!k&..J|
00000020  08 2d 7b 8e 82 4b 13 89  0f 5f a5 e7 a8 a3 52 c6  |.-{..K..._....R.|
00000030  e6 86 33 d7 67 39 d6 a9  73 f7 14 99 f7 0b e3 00  |..3.g9..s.......|
00000040  39 5e 8e bb a9 a1 45 b8  00 ea a0 a8 8d f2 6e 73  |9^....E.......ns|
00000050  78 a2 4a e0 db 20 89 4e  18 9d e7 0f a8 cb 0f e1  |x.J.. .N........|
00000060  29 9e 9d d3 3f e2 8b 40  cc 2b e8 59 1d 57 cc 96  |)...?..@.+.Y.W..|
00000070  f9 16 76 d4 36                                    |..v.6|
00000075
00000000  23 08 36 31 86 55 d0 84  07 c4 4c 1b d8 49 fe 6a  |#.61.U....L..I.j|
00000010  1e 43 34 6d f1 e1 05 ff  41 3a 21 6b 26 00 f7 4a  |.C4m....A:!k&..J|
00000020  08 2d 7b 8e 82 4b 13 89  0f 5f a5 e7 a8 a3 52 c6  |.-{..K..._....R.|
00000030  e6 86 33 d7 67 39 d6 a9  73 f7 14 99 f7 0b e3 00  |..3.g9..s.......|
00000040  39 5e 8e bb a9 a1 45 b8  00 ea a0 a8 8d f2 6e 73  |9^....E.......ns|
00000050  78 a2 4a e0 db 20 89 4e  18 9d e7 0f a8 cb 0f e1  |x.J.. .N........|
00000060  29 9e 9d d3 3f e2 8b 40  cc 2b e8 59 1d 57 cc 96  |)...?..@.+.Y.W..|
00000070  f9 16 76 d4 36                                    |..v.6|
00000075
```

DPR DMA performance – Virtex5

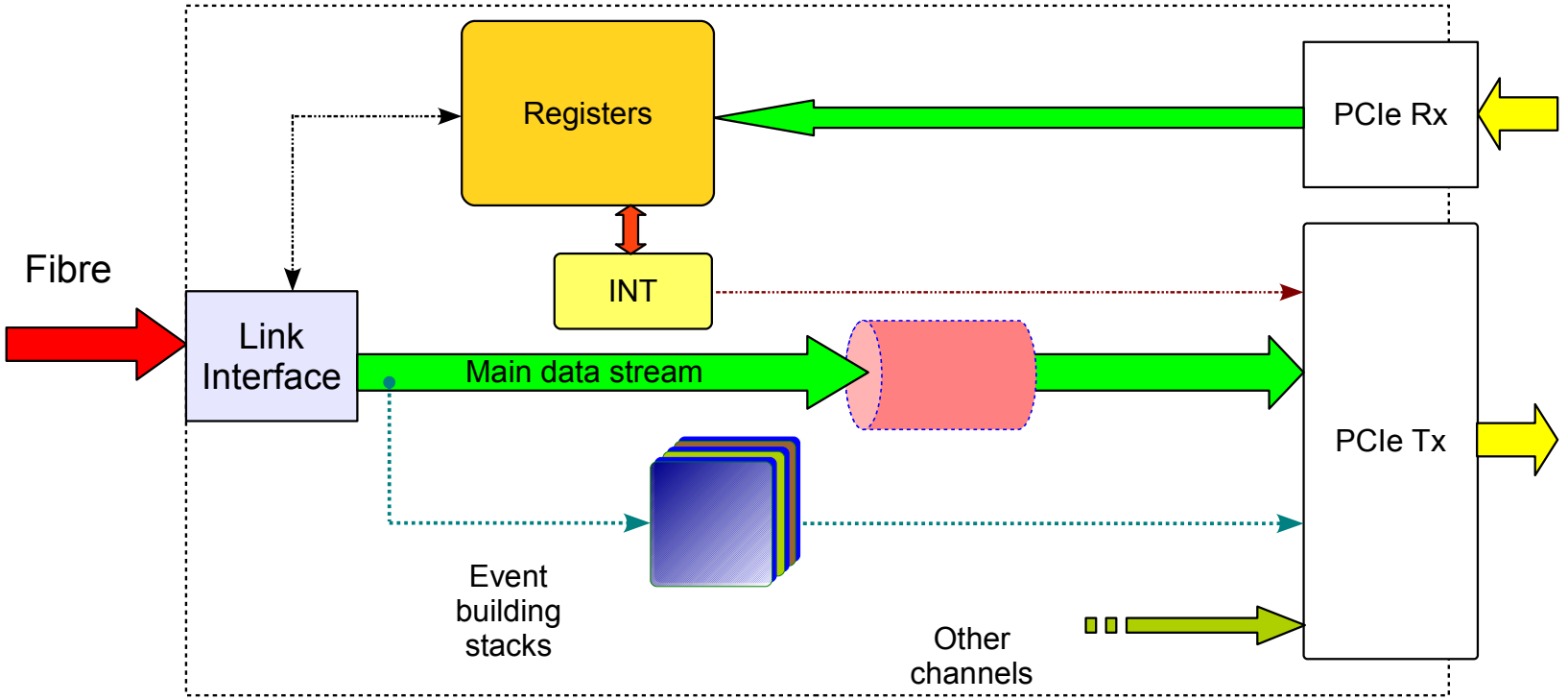


DPR DMA performance – Virtex6



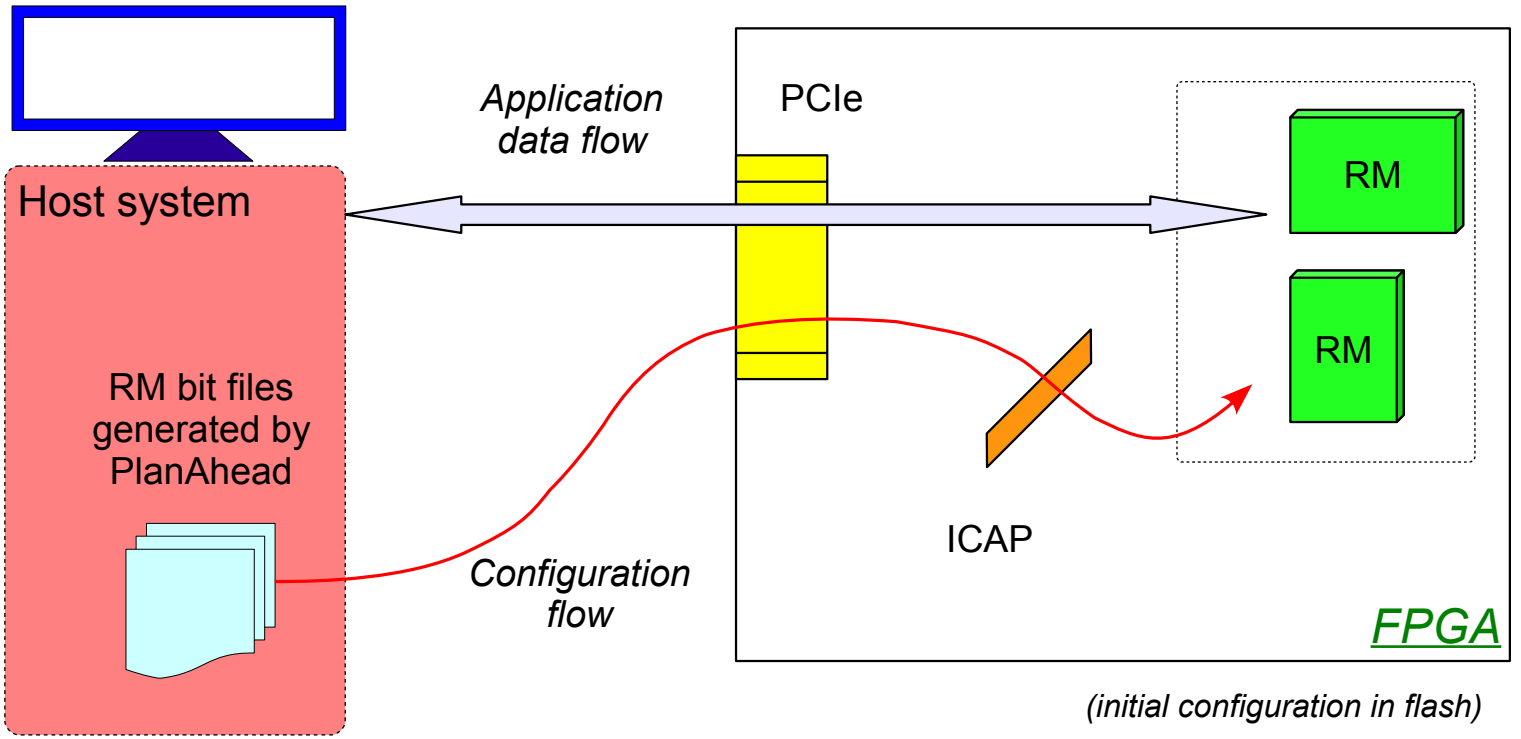
Pair experiments over.

Application scenario – A



- DPR firmware library for event building on ABB2
- Data reorder is compute in playing the marker finding logic

Application scenario – B



- A simplified reconfigurable accelerating card

Application scenario – C

?

Summary

- Towards generalized acceleration
  - Swift generation of partial bit files
    - PlanAhead
    - …
  - Internal port to access the configuration matrix
    - ICAP
  - High-speed data path to transfer dynamic partial bit files and application data
    - PCIe
    - HT
    - GbE
    - …
- No noticeable penalty upon DMA performance
- *Resource consumption bigger and timing constraints tighter. PR user guide (v12.3) states*
  - *expect 10% degradation in clock frequency*
  - *expect to not exceed 80% slices in packing density*

Next move

- Compressing the initial bit file for a faster boot
- DPR operation into MPRACE
- Event building firmware package on Virtex5 (AVNET)
- Automatic boundary decoupler

Xilinx Partial Reconfiguration User Guide (*V12.3*)

- ... it is very important to register the partition boundaries, and to use enables with these registers. During reconfiguration, the activity in these regions is indeterminate and could lead to design corruption if the output of the reconfiguring logic is used. Therefore, you should register boundaries with enables to disable the reconfigurable region during reconfiguration.
- ... the additional restrictions that are required for silicon isolation are expected to have an impact on most designs. In general,
  - Expect 10% degradation in Clock Frequency.
  - Expect to not exceed 80% slices in Packing Density.